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TITLE: METHOD FOR MANUFACTURING COMPOSITE SEMICONDUCTOR DEVICE

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ABSTRACT:

PROBLEM TO BE SOLVED: To uninformize characteristics by a method wherein a
semiconductor element is fixed to a composite semiconductor device substrate
with resin to be flatted, and the substrate of an assembly jig is detached from
the composite semiconductor device substrate.

SOLUTION: An assembly jig 10 is attached to semiconductor elements 4A, 4B. An
adhesive layer 5 is formed on a face, and marks of the semiconductor elements
4A, 4B conform to positions of marks 3, 3' of a substrate 1

so that they are arranged, pressed and connected. On a substrate 21 of a composite semiconductor device 20, polyimide resin 22 is applied more thickly than thicknesses of the semiconductor elements 4A, 4B. The assembly jig 10 is counter to the composite semiconductor device 20, which is applied static pressure while the polyimide resin is hardened, and the substrate 1 of assembly jig is separated. Thereby, a wire dimension is reduced and the composite semiconductor device can be arranged with high density and high precision.

L Number	Hits	Search Text	DB	Time stamp
1	6828	(wafer or (silicon adj substrate)) with die	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 19:32
2	2015	((wafer or (silicon adj substrate)) with die) and (die with (pad or pads))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 19:32
3	6567	wafer with die	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 19:32
4	1917	(wafer with die) and (die with (pad or pads))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 19:33
5	1889	((wafer with die) and (die with (pad or pads))) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:09
6	793	(((wafer with die) and (die with (pad or pads))) and (@ad<20011231)) and (ball or bump)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:07
7	10	6043109.URPN.	USPAT	2002/08/21 20:02
8	149	(die with wafer) and ((redistribution or circuit) near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:17
9	148	((die with wafer) and ((redistribution or circuit) near layer)) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:22
10	4742	(wafer with die) and (redistribution or circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:18
12	149	(wafer with die) and ((redistribution or circuit)near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:19
13	1	("6004867").PN.	USPAT	2002/08/21 20:22
14	9	6004867.URPN.	USPAT	2002/08/21 20:21
15	68	csp and ((redistribution or circuit) near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:40
16	65	(csp and ((redistribution or circuit) near layer)) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:44
17	751	257/777.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:40

18	32	257/777.ccls. and ((redistribution or circuit) near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:23
19	61	257/778.ccls. and ((redistribution or circuit) near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:44
20	61	(257/778.ccls. and ((redistribution or circuit) near layer)) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:56
21	114	257/777.ccls. and ((interposer or dielectric) and (ball or bump))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:55
22	167	257/777.ccls. and ((interposer or dielectric) and (ball or bump or trace or pad))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 20:56
23	167	(257/777.ccls. and ((interposer or dielectric) and (ball or bump or trace or pad))) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:16
24	2	"09260581"	JPO; DERWENT	2002/08/21 21:15
25	38	(die with mount) same ((silicon adj substrate) or wafer)	JPO; DERWENT	2002/08/21 21:26
26	120	(die with mount) same ((silicon adj substrate) or wafer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:16
27	119	((die with mount) same ((silicon adj substrate) or wafer)) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:33
28	27	MEMS and ((redistribution or circuit) near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:26
29	1821	(die or chip) near ((silicon adj substrate) or wafer)	JPO; DERWENT	2002/08/21 21:26
30	8	((die or chip) near ((silicon adj substrate) or wafer)) and (((redistribution or circuit) near layer) or interposer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:44
31	663	wafer with trace	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:33
32	653	(wafer with trace) and (@ad<20011231)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:33
33	6567	(wafer with die) and (chip or die)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:34

34	212	((wafer with trace) and (@ad<20011231)) and (chip or die)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:44
35	226	(silicon near carrier) and (chip or die)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:44
36	14	((silicon near carrier) and (chip or die)) and (((redistribution or circuit) near layer) or interposer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:45
37	12	(stacked adj wafer) and (((redistribution or circuit) near layer) or interposer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/08/21 21:46